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10/824,073	04/13/2004	Christopher J. Diorio	6928P009	6999

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EXAMINER	
SUAREZ, FELIX E	
ART UNIT	**PAPER NUMBER**
2857	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/824,073	Applicant(s) DIORIO ET AL.
	Examiner Felix E. Suarez	Art Unit 2857

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *18August2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 1-26, are rejected under 35 U.S.C. 102(b) as being unpatentable over Shanks et al. (U.S. Patent No. 6,784,813).

With respect to claims 1, 11, 21 and 26, Shanks et al. (hereafter Shanks) teaches a radio-frequency identification (RFID) circuit (a method, or a machine-readable medium) for use in an RFID tag, the circuit including:

an oscillator (see col. 45, lines 13-21); and

a tag controller to select a selected calibration value (see col. 17, lines 19-24 and col. 45, lines 22-38 and lines 51-67), from a plurality of calibration values stored within a memory structure associated with the RFID circuit (see col. 16 line 62 to col. 17 line 18), according to a first selection criterion, each of the calibration values corresponding to a respective oscillation frequency of the oscillator of the RFID circuit (see col. 45 line 65 to col. 46 line 24),

wherein the oscillator is operationally calibrated utilizing the selected calibration value (see col. 47 line 43 to col. 48 line 2).

With respect to claims 2, 12 and 22, Shanks further teaches that, the tag controller (see col. 17, lines 19-24) is to receive at least one calibration command (see col. 44, lines 56-65), and an associated update value, and to store at least one of the plurality of calibration values within the memory structure responsive to the at least one calibration command (see col. 47 line 61 to col. 48 line 3 and col. 50, lines 24-33).

With respect to claims 3, 13 and 23, Shanks further teaches that, the tag controller is to generate at least a first calibration value of the plurality of calibration values within the RFID circuit, and wherein the update value is a modification value by which a second calibration value, previously generated within the RFID circuit, is modified by the tag controller to generate the first calibration value (see col. 47 line 67 to col. 48 line 36).

With respect to claims 4, 14 and 24, Shanks further teaches that, the tag controller is to at least one of increment and decrement the second calibration value by the modification value to thereby generate the first calibration value (see col. 48, lines 22-36).

With respect to claims 5, 15 and 25, Shanks further teaches that, the update value is equal to the first calibration value, the update value having been generated in a calibration device external to the RFID tag (see col. 47 line 61 to col. 48 line 3 and col. 49, lines 51-66), and wherein the tag controller is to store the update value as the first calibration value within the memory structure (see col. 6, lines 54-59 and col. 50, lines 23-33).

With respect to claims 6 and 16, Shanks further teaches that, the first selection criterion includes any one of a group of selection criterion including a mode of operation of the RFID tag, a selection command received at the RFID tag (see col. 5, lines 50-67), an ambient condition applicable to the RFID tag (see col. 6 line 65 to col. 7 line 12), and an internal voltage applicable to the RFID tag (see col. 14, lines 39-50).

With respect to claims 7 and 17, Shanks further teaches that, the tag controller is to determine at least one of the plurality of calibration values based

on a radio-frequency signal received at the RFID tag from an RFID reader, and to store the at least one calibration value in the memory structure (see col. 5, lines 50-57 and col. 6, lines 54-59).

With respect to claims 8 and 18, Shanks further teaches that, the memory structure includes a non-volatile memory and a volatile memory, at least one of the plurality of calibration values being stored within the non-volatile memory, and at least a further one of the plurality of calibration values being stored within the volatile memory (see col. 6, lines 54-59).

With respect to claims 9 and 19, Shanks further teaches that, the at least one calibration value stored in the non-volatile memory is not related to a frequency of a radio-frequency signal received at the RFID tag from an RFID reader (see col. 6 line 60 to col. 7 line 12), the oscillator utilizing the at least one calibration value stored in the non-volatile memory to generate a modulator clock signal to be supplied to a modulator of the RFID circuit (see col. 17, lines 25-48).

With respect to claims 10 and 20, Shanks further teaches that, the at least one further calibration value stored in the volatile memory is derived from a radio-frequency signal received at the RFID tag from an RFID reader, the oscillator utilizing the at least one further calibration value to generate a

demodulation clock signal to be supplied to a demodulator of the RFID circuit (see col. 17, lines 25-48).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shanks et al. (U.S. Patent No. 6,784,813) in view of Parson (U.S. Patent No. 6,053,947).

With respect to claim 27, Shanks et al. (hereafter Shanks) teaches all the features of the claimed invention, except that Shanks does not teach

the description comprises a behavioral level description of the circuit.

But Parson teaches that, traditionally, circuits have been described using netlist languages, which are well known in the art. A netlist language is characterized by a number of constructs. First, a netlist language defines input and output ports of a subcircuit. A port is a connection to a subcircuit. Second, a netlist language represents connections between ports. Third, it can represent a nested subcircuit within a circuit. And fourth, a netlist language has some

measure of extension capability for tagging properties to ports, connections, and/or subcircuits.

Parson also teaches that, conventional netlist model languages used for simulating hierarchical circuits include, for example, structural VHDL (IEEE Standard VHDL Language Reference Manual, Std 1076-1993, IEEE, New York, 1993); and VERILOG (IEEE Standard 1364-1995) (see Parson; col.1, lines 30-45).

Parson also teaches that, the information of the source is a hierarchical netlist-behavioral model and the former takes the form of VHDL structural information and the latter the form of VHDL behavioral model (see Parson; col. 13, lines 10-19).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Shanks to include a conventional netlist model language as taught by Parson, because the conventional netlist model languages of Parson allows to use VHDL or VERILOG behavioral model format for simulating hierarchical circuits.

With respect to claim 28, Shanks teaches all the features of the claimed invention, except that Shanks does not teach

wherein the behavioral level description is compatible with a VHDL format.

But Parson teaches that, traditionally, circuits have been described using netlist languages, which are well known in the art. A netlist language is characterized by a number of constructs. First, a netlist language defines input and output ports of a subcircuit. A port is a connection to a subcircuit. Second, a netlist language represents connections between ports. Third, it can represent a nested subcircuit within a circuit. And fourth, a netlist language has some measure of extension capability for tagging properties to ports, connections, and/or subcircuits.

Parson also teaches that, conventional netlist model languages used for simulating hierarchical circuits include, for example, structural VHDL (IEEE Standard VHDL Language Reference Manual, Std 1076-1993, IEEE, New York, 1993); and VERILOG (IEEE Standard 1364-1995) (see Parson; col.1, lines 30-45).

Parson also teaches that, the information of the source is a hierarchical netlist-behavioral model and the former takes the form of VHDL structural information and the latter the form of VHDL behavioral model (see Parson; col. 13, lines 10-19).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Shanks to include a conventional netlist model language as taught by Parson, because the conventional netlist model languages of Parson allows to use VHDL behavioral model format for simulating hierarchical circuits.

With respect to claim 29, Shanks teaches all the features of the claimed invention, except that Shanks does not teach

wherein the behavioral level description is compatible with a Verilog format.

But Parson teaches that, traditionally, circuits have been described using netlist languages, which are well known in the art. A netlist language is characterized by a number of constructs. First, a netlist language defines input and output ports of a subcircuit. A port is a connection to a subcircuit. Second, a netlist language represents connections between ports. Third, it can represent a nested subcircuit within a circuit. And fourth, a netlist language has some measure of extension capability for tagging properties to ports, connections, and/or subcircuits.

Parson also teaches that, conventional netlist model languages used for simulating hierarchical circuits include, for example, structural VHDL (IEEE Standard VHDL Language Reference Manual, Std 1076-1993, IEEE, New York, 1993); and VERILOG (IEEE Standard 1364-1995) (see Parson; col.1, lines 30-45).

Parson also teaches that, the simulators used can be any traditional simulator such as VERILOG (see Parson; col. 5 line 65 to col. 6 line 7).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Shanks to include a conventional netlist

model language as taught by Parson, because the conventional netlist model languages of Parson allows to use a VERILOG simulation model format for simulating hierarchical circuits.

With respect to claim 30, teaches all the features of the claimed invention, except that Shanks does not teach

the description comprises a register transfer level netlist.

But Parson teaches that, traditionally, circuits have been described using netlist languages, which are well known in the art. A netlist language is characterized by a number of constructs. First, a netlist language defines input and output ports of a subcircuit. A port is a connection to a subcircuit. Second, a netlist language represents connections between ports. Third, it can represent a nested subcircuit within a circuit. And fourth, a netlist language has some measure of extension capability for tagging properties to ports, connections, and/or subcircuits.

Parson also teaches in circuit schematic hierarchy that, each subcircuit has a type name followed by an instance name, and in addition to the boundary ports register houses three 16-bit registers. Each processor instruction can supply one of the three registers from within register or sigin as a source operand (see Parson; col. 17, lines 36-45).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Shanks to include a circuit schematic

hierarchy as taught by Parson, because the circuit schematic hierarchy of Parson allows to use a hierarchical register netlist; as desired.

With respect to claim 31, teaches all the features of the claimed invention, except that Shanks does not teach,

the description comprises a transistor level netlist.

But Parson teaches that, traditionally, circuits have been described using netlist languages, which are well known in the art. A netlist language is characterized by a number of constructs. First, a netlist language defines input and output ports of a subcircuit. A port is a connection to a subcircuit. Second, a netlist language represents connections between ports. Third, it can represent a nested subcircuit within a circuit. And fourth, a netlist language has some measure of extension capability for tagging properties to ports, connections, and/or subcircuits.

Parson also teaches that, a circuit schematic hierarchy provides the top level of design hierarchy for a particular circuit named alupipe. It has four boundary ports: rst, clk, sigin and sigout. At the outermost level alupipe works by reading sigin, transforming its value according to a stored program, and writing output to sigout (see Parson; col. 17, lines 26-35).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Shanks to include a circuit schematic

hierarchy as taught by Parson, because the circuit schematic hierarchy of Parson allows to use a hierarchical netlist for a particular circuit; as desired.

Conclusion

Prior Art

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dieska et al. [U.S. Patent No. 5,912,632] describes a passive RF tag with a tag oscillator.

Loyer et al. [U.S. Patent No. 6,687,293] describes a circuit that calculates the relative relationship between an internal oscillator of the RFID tag device and an external PPM source as a RFID tag reader.

Lee et al. [U.S. Patent No. 6,700,931] describes a RFID tag reader.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Felix Suarez, whose telephone number is (571) 272-2223. The examiner can normally be reached on weekdays from 8:30 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular communications and for After Final communications.

January 17, 2006

F.S.

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